



Electronic Parts Evaluation Activities

at

JPL

4/26/2000

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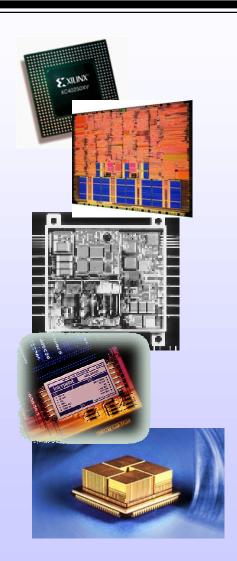
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Overview



- Evaluate and assess new and advanced microelectronics device technologies for application in high reliability systems
 - Identify common failure modes and mechanisms of new technologies
 - Evaluation and characterization of new device Technologies
 - Provide an infusion path for advanced technologies
 - Develop innovative and cost effective reliability and qualification methods
- Develop a new strategic alliances with industry, academia, and other government agencies for evaluation activities





Parts Challenges



Technical challenges

- Smaller feature sizes and miniaturization
- Low power devices and processes
- Device complexity
- Radiation Tolerance of commercial Processes

Environmental challenges

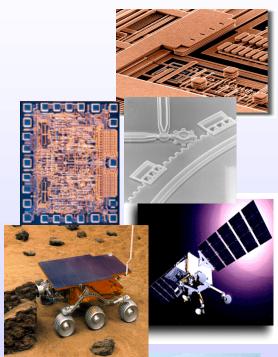
- Operation at extreme temperatures
- Reduction in mass and volume
- New radiation effects and high radiation environments

Programmatic challenges

- Fast, better, cheaper missions
- 1/2 the cycle time, 2/3 the cost

Industry challenges

- * Diminishing Hi-Rel suppliers
- No supporting military infrastructure and standards
- No procurements for small volume



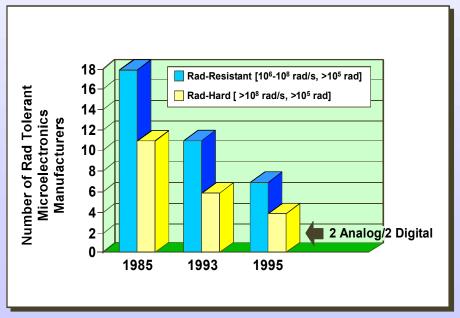




Diminishing Hi-Rel Suppliers



- Military/space market represents too small a customer to drive new technology development
- Diminishing Hi-Rel suppliers means
 - No high-performance and high-reliability parts
 - No standard on screening/qualification
 - No rad-hard parts/processes
- Focus on assessing new technologies and electronic parts to understand the following for Hi-Rel applications
 - More electrical characterizations
 - Upscreening and qualification tests
 - Identification of dominant failure modes for various requirements
 - Radiation characterization tests
 - Material characteristics
 - Reliability of advanced technology devices for extreme environments
 - Reliability and quality assurance standards for highly reliable parts

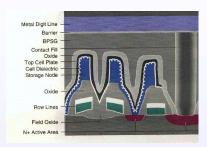


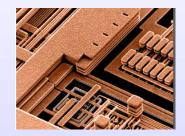


COTS Evaluations



- The miniaturization and commercialization trends are the driving force for usage of COTS for space flight projects
- The challenge is to use COTS in high radiation and reliability requirements
 - Identify the reliability and validate COTS for flight projects
 - Evaluation of SDRAMs, EEPROMs, Flash Memories for high temperature and high radiation environments
 - Evaluation of various discretes, passives, linear devices
 - Provide upscreening options for projects with a variety of risk levels for using COTS devices
 - Provide KGD requirements for insuring reliability of COTS devices for fight projects









COTS Evaluations (cont.)



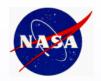
PEMS

- Establish validation methods for plastic (PEM) parts
- Develop tailored upscreen procedure for insuring reliable PEMs in JPL Flight projects
- Develop a baseline approach for reliability assurance for space flight applications
- Enable flight projects to use state-of-theart devices not otherwise available
- Need to develop of new strategic alliances with industry, academia, and other government agencies to leverage resources for COTS reliability/qualification evaluations





http://cots.jpl.nasa.gov/



DC/DC Converters



Objective

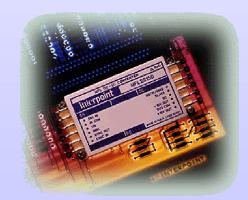
- Identify and publish a list of preferred DC/DC converter suppliers and technologies for space application
- Evaluate reliability of DC/DC converters and publish reliability assurance guidelines

Status

- Completed evaluation reports from on-site supplier line evaluations,
 DPA, and other environmental testing
- Produced summary matrix for DC/DC converter selection criteria

Plan

Generate listing of preferred/qualified suppliers





Reliability of Cu-Based Microelectronic Metallization Systems

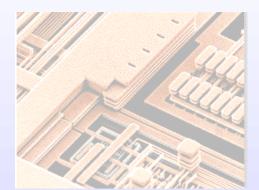


Objective

Evaluate reliability of Cu-based microelectronic metalization systems

Status

- Engineering studies of Cu/low-k systems
 - Expected failure mechanisms identified
 - Variability due to process seen as major issue
 - · Critical reliability detractors found
 - · Experiments identified
- Presented several papers in various conferences



Plan

- Publish a report on expected failure modes and mechanisms for Cu/low-k interconnect systems
- Provide recommendations for use and application of these materials in high reliability space flight systems



SOI Reliability



Objective

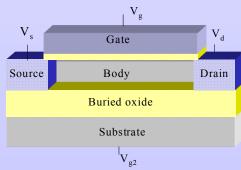
- Perform a comprehensive technology characterization of SOI Mixed Signal ASIC processes in partnership with industry, academia, and government-sponsored laboratories
- Provide critical information for design engineers and circuit designers relating to the characteristics and limitations of this new technology for high reliability applications (in an extended temperature range down to -150°C)

Status

- Completed low temperature evaluation of DC characteristics (300K to 77K) for 0.25-um FD-SOI transistors.
- Obtained preliminary proton radiation test results.

Plan

- Evaluate 0.18-um fully-depleted and 0.8-um partially-depleted devices for mixedsignal applications.
- Modify device parameters using simulation tools and, based on simulation results, fabricate devices with better performance in harsh environments.





Non-Volatile Memory (NVM) Evaluation



Objective

 Develop a test methodology for determination of non-volatile memory (NVM) reliability and radiation effects and construction of a test structure for characterization.

Status

- Characterization of all major NVM types:
 - Floating gate technology: including PROM, UVPROM, EEPROM, PLED, and flash technologies
 - Ferroelectric technology: including GMRAM, FeRAM, Spin Valve, and PZT technologies
 - Phase Change Materials Technology: including Chalcogenide and Antifuse technologies

Plan

- Develop test structures and methodology for testing of NVM:
 - Reliability and operational liability of NVM
 - · Radiation effects and mitigation strategies
 - Develop NVM characterization test database from existing data and test matrix required for complete characterization



KGD for Space Applications



Objective

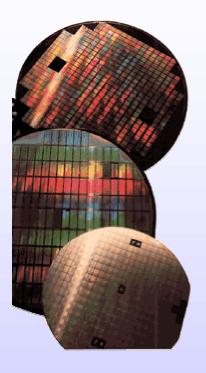
 Establish all requirements for semiconductor KGD which are purchased by JPL or its subcontractors for use in JPL flight projects

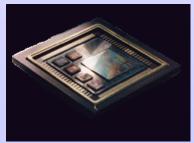
Status

- Developed guidelines for insuring two level KGD in JPL flight hardware and an operating procedure for die storage and handling
- Collected and reviewed KGD test methods, KGD vendor programs, KGD test options, and risk associated with KGD screens/options

Plan

Facilitate future die procurements, infusion, and usage







Electronics For Extreme Environments



Objective

 Develop reliability assessments of electronic parts at extreme environments and identify failure mechanisms to support future JPL/NASA flight projects

Status

- Conducted characterization tests on a number of parts in support of JPL flight projects at low temperature (-170 C)
- Report "Failure Mechanisms In Electronic Devices At Low Temperatures Part I: Electrically Induced Failures"
- Report on Failure Mechanisms In Electronic Devices At Low Temperatures, Part II: Mechanically Induced Failures: "Thermo-Mechanical Stress Induced Failures in Die Metallization Lines – an Overview"
- Report "Die Attachment For -120 C To +20 C Thermal Cycling Of Microelectronics For Future Mars Rovers - An Overview"

Plan

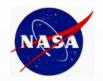
 Support the Mars Program in test and characterization of commercial encoder boards for low temperature applications



Other Parts Evaluation Activities



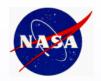
- Radiation Effects
- MEMS Reliability
- Compound Semiconductor Reliability
- SiGe Reliability
- Optoelectronic And Photonic Devices
- InP Reliability Characterization
- TEM as a Reliability Tool
- Specific parts Evaluations



Summary



- COTS insertion into high reliability space systems requires detailed knowledge of the performance and characteristics of these components in a space environment
- A systematic approach to the "qualification" of COTS components is a must
- Understanding the technology and the intended application are essential first steps of qualification
- There is a clear need to leverage resources and develop strategic alliances for the evaluation and characterization of COTS components for high reliability applications.



Acknowledgement



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